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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,071	12/21/1999	TONGBI JIANG	MICRON.110A	6968

20995 7590 10/23/2002

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EXAMINER	
ALCALA, JOSE H	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AD

Office Action Summary	Application No.	Applicant(s)	
	09/471,071	JIANG, TONGBI	
	Examiner	Art Unit	
	Jose H Alcala	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on *12 March 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 3/12/02 have been disapproved. The proposed drawing changes are clearing all the objections to the drawings, except the objection to the crosshatching. The changes made to the crosshatching are still confusing and they do not follow the patterns of MPEP 608.02. For that reason all the objections to the drawings are maintained.

A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

2. Figures are improperly crosshatched. All of the parts shown in the section, and only those parts, must be crosshatched. The elements which are made of metal need to have a different crosshatching than the elements which are dielectric, using the crosshatching patterns, shown in the MPEP section below. The crosshatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 21-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: How the flexible tape is located in relation to the solder ball array and the adhesive layer.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8-23,25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the publication: "Tessera's Micro ball Grid Array, Chapter 16".

Regarding Claim 8, Tessera teaches an integrated circuit package (Figure 16.2), comprising: a die (labeled as chip on figure 16.2); a die attach layer over the die

(labeled as elastomeric compliant layer); and an array of solder balls (see page 260 lines 21-22) over the die attach layer. See figure 16.2.

Tessera fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 106 ppm/°C , as taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate.

Regarding Claim 9, Tessera teaches a flexible tape (labeled as Fan-in Tab leads in figure 16.2) connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

Regarding Claim 10, Tessera teaches that the die attach layer has a thickness of between about 5 and 7 mils (See page 260, lines 3-4).

Regarding Claim 11, Tessera teaches that the die attach layer is an epoxy modified with elastomeric material (See page 260, lines 2-3).

Regarding Claim 12, Tessera teaches that the array is a ball grid array (see page 260 lines 21-22).

Regarding Claim 13, Tessera teaches that the array is a tape ball grid array. (See figure 16.2).

Regarding Claim 14, Tessera teaches that the array is a micro ball grid array. (See description of figure 16.2, in page 261).

Regarding Claim 15, Tessera teaches an integrated circuit package (Figure 16.2), comprising: a die (labeled as chip on figure 16.2); a die attach layer over the die (labeled as elastomeric compliant layer); and an array of solder balls (see page 260 lines 21-22) over the die attach layer. In addition Tessera teaches that the die attach layer is an elastomeric compliant layer, therefore it is inherent that it has a modulus of elasticity of less than about 126 ksi. See figure 16.2.

Tessera fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 106 ppm/°C , as taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate.

Regarding Claim 16, Tessera teaches a flexible tape (labeled as Fan-in Tab leads in figure 16.2) connecting the array of solder balls to the die, wherein one end of

the tape is located over the die attach layer, and another end of the tape is located over the die.

Regarding Claim 17, Tessera teaches a first level integrated circuit package (Figure 16.2) comprising: a first level package including a chip (labeled as chip on figure 16.2); an array of solder balls (see page 260 lines 21-22), an adhesive layer (labeled as elastomeric compliant layer) between the chip and the array of solder balls, and a flexible tape (labeled as Fan-in Tab leads in figure 16.2) connecting the array to the chip wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip. The limitation that the array of solder balls is: "for connecting the first level package to a second level package", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Tessera fails to explicitly teach that the adhesive layer has a coefficient of thermal expansion of less than about 200 ppm/°C, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the adhesive layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 200 ppm/°C , as

taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate.

Regarding Claim 18, Tessera teaches that the tape connects the array to the chip using μBGA technology.

Regarding Claim 19, Tessera fails to explicitly teach that the adhesive layer has a coefficient of thermal expansion of less than about 150 ppm/°C, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 150 ppm/°C , as taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate.

Regarding Claim 20, Tessera fails to explicitly teach that the adhesive layer has a coefficient of thermal expansion of less than about 100 ppm/°C, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the die attach layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 100 ppm/°C , as

taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate.

Regarding Claim 21, Tessera teaches a first level integrated circuit package (Figure 16.2) comprising: a first level package including a chip (labeled as chip on figure 16.2); an array of solder balls (see page 260 lines 21-22), an adhesive layer (labeled as elastomeric compliant layer) between the chip and the array of solder balls, and a flexible tape (labeled as Fan-in Tab leads in figure 16.2) connecting the array to the chip wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip. In addition Tessera teaches that the adhesive layer is an elastomeric compliant layer, therefore it is inherent that it has a modulus of elasticity of less than about 126 ksi. See figure 16.2.The limitation that the array of solder balls is: "for connecting the first level package to a second level package", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Tessera fails to explicitly teach that the adhesive layer has a coefficient of thermal expansion of less than about 200 ppm/°C and a modulus of elasticity of greater than about 10 ksi, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate, and a lower package stiffness to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the

art at the time the invention was made to make the adhesive layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 200 ppm/°C, as taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate. In addition, it would have been further obvious to have a modulus of elasticity greater than about 10 ksi, in order to make the layer having the desired stiffness to relieve the stresses due to thermal mismatch between a chip and a substrate. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claims 22 and 23, Tessera fails to explicitly teach that the adhesive layer has a modulus of elasticity of greater than about 50 ksi, and greater than about 100 ksi, respectively. Tessera teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate, and a lower package stiffness to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the adhesive layer having a thermal expansion coefficient as close as possible to the chip and to the substrate and a modulus of elasticity greater than about 50 or than about 100 ksi, in order to make the layer having the desired stiffness to relieve the stresses due to thermal mismatch between a chip and a substrate. In addition, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claim 25, Tessera teaches an integrated circuit package (Figure 16.7), comprising: a flexible substrate (see Figure 16.7, and page 261, lines 20-22); a chip (labeled as silicon die in figure 16.7); a plurality of conductive terminals on the substrate (See terminals in Figure 16.7); a plurality of conductive leads (labeled as compliant lead in figure 16.7) electrically connecting the conductive terminals to the chip; and a compliant material (labeled as compliant polymer/elastomer in Figure 16.7) between the chip and the substrate.In addition Tessera teaches that the compliant material is an elastomeric compliant layer, therefore it is inherent that it has a modulus of elasticity of less than about 126 ksi.

Tessera fails to explicitly teach that the adhesive layer has a coefficient of thermal expansion of less than about 200 ppm/°C, but teaches that it is known to have a compliant layer having a thermal expansion coefficient compliant to the chip and substrate, and a lower package stiffness to relieve the stresses due to thermal mismatch between a chip and a substrate as set forth in page 264, lines 2-10 and page 265, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the adhesive layer having a thermal expansion coefficient as close as possible to the chip and to the substrate which would inherently be less than about 200 ppm/°C, as taught by Tessera in order to relieve the stresses due to thermal mismatch between a chip and a substrate. In addition, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claim 26, Tessera teaches that the plurality of conductive terminals includes an array of solder balls (See Figure 16.7).

Regarding Claim 27, Tessera teaches that the plurality of conductive leads includes TAB leads (See page 265, lines 22-25)

Regarding Claim 28, Tessera teaches that the flexible substrate is a polyimide (See page 259, lines 22-23).

Response to Arguments

7. Applicant's arguments with respect to claims 8-23,25-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention or some similar arrangements of the elements: King et al. (US Patent No. 5,677,566), Suzuki (US Patent No. 6,049,038), Suzuki (US Patent No. 5,650,918), Khandros et al. (US Patent No. 5,347,159) and Bridges et al. (US Patent NO. 4,816,426).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
October 20, 2002

A. Paladini 10-21-02
ALBERT W. PALADINI
PRIMARY EXAMINER